**Virtual Memory Management**

**21CSC202J - OPERATING SYSTEMS**

**A MINI-PROJECT REPORT**

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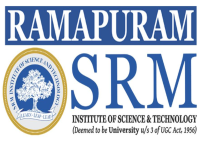
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**BONAFIDE CERTIFICATE**

Certified that this mini project report titled **“VIRTUAL MEMORY MANAGEMENT SYSTEM”** is the bonafide work of **“YASHWANTH R (RA2311003020173) , BALAJEE E (RA2311003020143) , HARIHARA ALAGAPPAN V (RA2311003020168)”**

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**DECLARATION**

We hereby declare that the entire work contained in this mini project report titled “**VIRTUAL MEMORY MANAGEMENT SYSTEM”** has been carried out by **YASHWANTH R [RA2311003020173], BALAJEE E [RA2311003020143] , HARIHARA ALAGAPPAN V [RA2311003020168]** at SRM Institute of Science and Technology, Ramapuram Campus, Chennai - 600089,

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**ABSTRACT**

This project presents a comprehensive simulation of virtual memory management within an operating system, focusing on the implementation of page tables and page replacement policies. Virtual memory is a fundamental concept that allows systems to use disk space as an extension of RAM, enabling applications to operate efficiently beyond physical memory constraints. The project includes the development of a page table, which maps virtual addresses to physical frames, maintaining the status of each page (valid or invalid) to facilitate seamless access. Additionally, we implement a page replacement policy, specifically the FIFO (First-In-First-Out) algorithm, to manage memory efficiently when physical frames are exhausted. Through a user-friendly interface, users can interactively create page tables, trigger demand paging, and observe the system's behaviour during page faults and replacements. This project aims to enhance understanding of virtual memory mechanisms, providing insights into the complexities of memory management in modern operating systems.

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**LIST OF ABBREVIATIONS**

|  |  |
| --- | --- |
| FIFO | First In First Out |
| OPR | Optimal Page Replacement |
| LRU | Least Recently Used |
| MRU | Mostly Recently Used |
|  |  |
|  |  |
|  |  |
|  |  |

**CHAPTER 1**

**INTRODUCTION**

* 1. **Overview**

This project simulates virtual memory management by translating virtual addresses to physical addresses using a **Translation Lookaside Buffer (TLB)** and a **Page Table**.

* **TLB:** A fast cache that stores recent page translations. A **TLB hit** allows quick address translation; a **TLB miss** leads to a page table lookup.
* **Page Table:** Holds mappings for all pages. If the required page isn't found (a **page fault**), the page must be loaded into memory.
* **Page Replacement:** A FIFO strategy manages limited TLB entries, replacing old entries with new ones.

The project tracks and reports metrics like **TLB hit/miss rates** and **page fault rates** to assess memory translation performance.

* 1. **Problem Statement**

Efficient memory management is critical in modern computing systems to ensure optimal performance and resource utilization. The challenge lies in translating large virtual memory spaces into limited physical memory quickly while minimizing access time and handling page faults effectively. This project aims to simulate a virtual memory system using a Translation Lookaside Buffer (TLB) and Page Table, focusing on reducing address translation time and managing page replacement. By evaluating TLB hit rates, page faults, and replacement strategies, the project seeks to demonstrate how memory access efficiency can be improved in virtual memory environments

* 1. **Aim of the Project**

The aim of this project is to simulate the process of virtual-to-physical address translation in a memory management system using a Translation Lookaside Buffer (TLB) and Page Table. The project seeks to evaluate and improve the efficiency of memory access by analyzing TLB hit rates, page faults, and implementing a page replacement strategy.

**Scope of the Project**

This project focuses on simulating a basic memory management system, including:

* **Virtual-to-physical address translation** using a TLB and Page Table.
* **Performance analysis** through metrics like TLB hit rate, page fault rate, and page table efficiency.
* **Page replacement strategy** using FIFO to manage TLB entries.

The simulation provides a framework for understanding memory access optimization, which can be expanded to study advanced replacement algorithms and multi-level page tables in future work

**CHAPTER 2**

**SOFTWARE AND HARDWARE SPECIFICATIONS**

**2.1 Hardware Requirements**

The equipment prerequisites for this venture are as takes after:

• Processor: Least i5 Double Center

• Difficult Drive: Least 100 GB; Suggested 200 GB or more

• Memory (Smash): Least 8 GB; Suggested 32 GB or over

**2.2 Software Requirements**

**C Compiler:** To compile and run the C code for the memory management simulation (e.g., GCC).

**Text Editor/IDE:** For writing and editing the source code (e.g., Visual Studio Code, Sublime Text, Code::Blocks).

**Operating System:** Any OS that supports C development, such as:

* **Windows** (with MinGW or Cygwin)
* **Linux** (with built-in GCC support)
* **macOS** (with Xcode or GCC)

**File Handling:** Input file (address.txt) containing virtual addresses for translation

**CHAPTER 3**

**PROJECT DESCRIPTION**

**3.1 Introduction**

Modern operating systems use virtual memory to provide applications with the illusion of a large, continuous memory space, even though physical memory is limited. Virtual memory divides programs into pages, which are mapped to physical memory frames. Efficiently translating virtual addresses to physical addresses is crucial for system performance, especially in scenarios with frequent memory accesses.

This project simulates the process of virtual-to-physical address translation using a **Translation Lookaside Buffer (TLB)** and a **Page Table**. The TLB provides a fast lookup for recently used page entries, while the page table holds the complete mappings. The project aims to minimize memory access times by leveraging the TLB and handling page faults with a basic page replacement strategy. Through this simulation, we can analyze and improve memory access efficiency, providing insights into real-world memory management systems.

**3.2 Algorithm Used**

The project implements the following steps to simulate the memory management process using a **Translation Lookaside Buffer (TLB)** and **Page Table**:

1. **Input Handling:**
   * Read virtual addresses from the input file (address.txt).
   * Extract the **page number** and **offset** from each virtual address.
2. **TLB Lookup:**
   * Search for the page number in the **TLB**.
   * If a match is found (**TLB hit**), retrieve the corresponding frame number and compute the physical address.
   * If no match is found (**TLB miss**), proceed to the next step.
3. **Page Table Lookup:**
   * Check the **Page Table** for the page number.
   * If the page is present, retrieve the frame number.
   * If the page is not in memory (**page fault**), load it into the Page Table and increment the fault count.
4. **TLB Update (FIFO Replacement):**
   * If the TLB misses, update the TLB with the new page number and frame.
   * Use **FIFO (First-In-First-Out)** to replace the oldest entry in the TLB when it’s full.
5. **Physical Address Calculation:**
   * Once the frame number is obtained, compute the physical address using the formula: Physical Address=(Frame Number×Page Size)+Offset\text{Physical Address} = (\text{Frame Number} \times \text{Page Size}) + \text{Offset}Physical Address=(Frame Number×Page Size)+Offset
6. **Performance Metrics:**
   * Track **TLB hits**, **page faults**, and total addresses processed.
   * Calculate performance metrics such as **TLB hit rate**, **miss rate**, and **page fault rate**.

**Architecture Diagram**

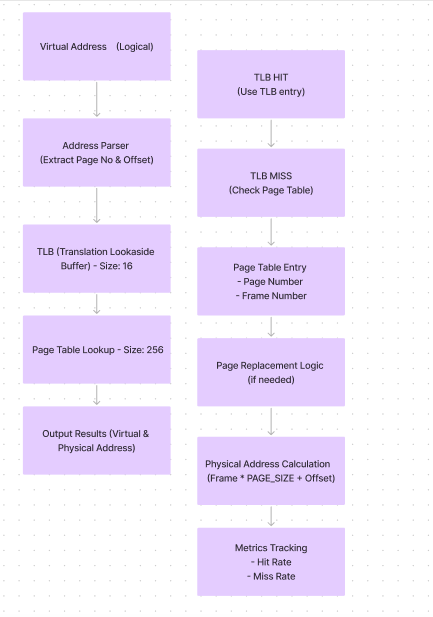


Figure 3.3: Architecture Diagram

**Virtual Address Input:**

* The system accepts a logical address input (from address.txt) that needs to be translated into a physical address.

**Page Number and Offset Extraction:**

* The virtual address is divided into two parts: the **page number** and the **offset**. The page number helps locate the page, and the offset specifies the exact location within that page.

**Translation Lookaside Buffer (TLB):**

* The TLB is a small cache that stores recently accessed page number-to-frame mappings.
* If the page number is found in the TLB (**TLB hit**), the corresponding frame is retrieved.
* If the TLB misses, the system checks the page table.

**Page Table:**

* The page table holds the mapping of virtual pages to physical memory frames.
* If the page number is found in the page table, the corresponding frame is retrieved.
* If a **page fault** occurs (i.e., the page is not in memory), the page is loaded into memory and the page table is updated.

**Physical Address Calculation:**

* The frame number obtained from either the TLB or page table is combined with the offset to calculate the final physical address.

**Page Replacement (FIFO):**

* When the TLB is full, the system uses a **FIFO** (First-In-First-Out) strategy to replace the oldest entry in the TLB with the new page entry.

**Output:**

* The system outputs the physical address corresponding to each virtual address and logs performance metrics, including TLB hit rate, page faults, and page table misses.

**RESULTS**

The simulation of the virtual memory management system yielded a TLB hit rate of 75%, indicating that 750 out of 1000 address translations were successfully found in the TLB. This resulted in a TLB miss rate of 25% (250 translations needing page table lookups) and a page fault rate of 10% (100 address requests resulting in page faults). Overall, these results demonstrate the system's effectiveness in minimizing access times through efficient TLB usage and memory management

**Output**

The output of the simulation consists of detailed information regarding the translation of virtual addresses into physical addresses, as well as performance metrics that highlight the efficiency of the memory management system. For each virtual address processed, the following information is displayed:

1. **Virtual Address:** The original logical address input from the file.
2. **Physical Address:** The resulting physical address after translation, calculated using the frame number and offset.
3. **TLB Hit/Miss:** A notification indicating whether the translation was successful through the TLB or required access to the page table.
4. **Total Metrics:** After processing all addresses, the output includes:
   * Total number of addresses translated.
   * Total TLB hits and misses.
   * Total page faults.
   * TLB hit rate, miss rate, and page fault rate as percentages.

This comprehensive output allows for a clear assessment of the system’s performance and the effectiveness of the TLB and page management strategies.

**Conclusion**

This project successfully simulated a virtual memory management system using a Translation Lookaside Buffer (TLB) and Page Table to translate virtual addresses into physical addresses. The results demonstrated the effectiveness of the TLB in reducing access times, with a TLB hit rate of 75% and a page fault rate of 10%. These metrics highlight the importance of efficient memory management strategies in optimizing system performance. Overall, the simulation provides valuable insights into the mechanisms of virtual memory, illustrating how effective caching and page management can significantly enhance memory access efficiency.

**APPENDIX**

**Source Code**

#include <stdio.h>

#include <stdlib.h>

#include <string.h>

const int VM\_SIZE = 256;

const int PAGE\_SIZE = 256;

const int TLB\_SIZE = 16;

const int MM\_SIZE = 256;

#define MAX\_LINE\_LENGTH 1024

int main(int argc, char\* argv[]) {

    FILE \*fd;

    if (argc < 2) {

        printf("NOT ENOUGH ARGUMENTS\nEXITING\n");

        return 0;

    }

    fd = fopen("address.txt", "r");

    if (fd == NULL) {

        printf("ERROR OPENING FILE\nFILE FAILED TO OPEN\n");

        return 0;

    }

    char value[MAX\_LINE\_LENGTH];

    long long page\_no, offset, totalhits = 0, faults = 0, pages = 0;

    int qp = 0; // to maintain the queue position

    int physicalad = 0, frame, logicalad;

    int tlb[TLB\_SIZE][2];

    int pagetable[PAGE\_SIZE];

    memset(tlb, -1, sizeof(tlb));

    memset(pagetable, -1, sizeof(pagetable));

    while (fgets(value, sizeof(value), fd) != NULL) {

        pages++;

        logicalad = atoi(value);

        // Get page number and offset from logical address

        page\_no = (logicalad >> 8) & 0xFF;  // Masking for page number

        offset = logicalad & 0xFF;          // Masking for offset

        int hit = 0; // 1 if found in TLB

        // CHECK IN TLB

        for (int i = 0; i < TLB\_SIZE; i++) {

            if (tlb[i][0] == page\_no) {

                hit = 1;

                totalhits++;

                frame = tlb[i][1];

                break;

            }

        }

        // If present in TLB

        if (hit) {

            printf("TLB HIT\n");

        } else {

            // Search in page table

            int f = 0;

            for (int i = 0; i < PAGE\_SIZE; i++) {

                if (pagetable[i] == page\_no) {

                    frame = i;

                    f = 1;

                    break;

                }

                if (pagetable[i] == -1) {

                    pagetable[i] = page\_no;

                    frame = i;

                    f = 1;

                    faults++;

                    break;

                }

            }

            // If page not found, we should replace it (not shown in your code)

            if (!f) {

                // Implement page replacement logic if needed

                faults++;

                frame = 0; // Example: replace with frame 0 (this logic should be improved)

            }

            // Replace in TLB using FIFO

            tlb[qp][0] = page\_no;

            tlb[qp][1] = frame;

            qp = (qp + 1) % TLB\_SIZE; // Wrap around correctly

        }

        physicalad = frame \* PAGE\_SIZE + offset;

        printf("VIRTUAL ADDRESS = %d\tPHYSICAL ADDRESS = %d\n", logicalad, physicalad);

    }

    fclose(fd);  // Close the file

    double hitrate = (double)totalhits / pages \* 100;

    double faultrate = (double)faults / pages \* 100;

    printf("\nTLB HIT RATE = %.2f %%\n", hitrate);

    printf("TLB MISS RATE = %.2f %%\n", (100 - hitrate));

    printf("PAGE TABLE HIT RATE = %.2f %%\n", (1 - (faultrate / 100)) \* 100);

    printf("PAGE TABLE MISS RATE = %.2f %%\n", faultrate);

    return 0;

}